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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,435	12/23/1999	MICHAEL J. MCTAGUE	INTL-0296-US	7390

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ART UNIT	PAPER NUMBER
2631	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/471,435	MCTAGUE ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 14-30* is/are rejected.

7)☒ Claim(s) *2,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 01/19/2004 has been entered. Claims 1-30 are pending in this Office action.

Response to Arguments

2. Applicant's arguments filed on 01/19/2004 have been fully considered but they are not persuasive.

- Applicant argues on page 2 that Gockler reference fails to teach or suggest an asymmetric digital subscriber loop (ADSL) modem including an integrated circuit with use of a multiplexer to multiplexer the lower data rate data and control information such that the lower data rate data and control information are transmitted externally off the integrated circuit.

On the contrary with Applicant's argument, Gockler teachings establish prima facie obvious case of claim 1. As known in the art that components of a modem are normally implemented on an integrated circuit even though Gockler reference does not expressly disclose the modem including an integrated circuit. It has also admitted on page 2 lines 15-17 in the background of the patent application that existing ADSL modems generally are implemented using two or more integrated circuits. Hence, one of ordinary skill in the art will appreciate that Gockler modem inherently includes an integrated circuit as stated in previous rejection.

Gockler modem has two transmitting channels and two receiving channels, and *signal transmission in the modem takes place via only one of the two transmitting channels or receiving channels*, see Gockler reference column 1, lines 54-62. As argued by the Applicant, the multiplexer in Gockler reference receiver receives outputs from two decoders instead of receiving lower data rate data and control information. Nevertheless, as recited above, signal transmission in the modem takes place via only one of the two transmitting channels or receiving channels. More specifically, see Gockler reference figure 2, it is true that the multiplexer in Gockler reference receives outputs from two decoders, however, the multiplexer MUX only multiplexes one receiving channel in constrast with Applicant's assertion that the multiplexer in Gockler reference uses outputs from both decoders. Furthermore, synchronization circuits SYNC 1 and SYNC2 are located in the two received signal paths to synchronize the circuits in the respective signal path to the carrier frequency, carrier phase, and sampling cycle of the received data signal, see Gockler reference figure 2. In that manner, one of ordinary skill in the art will appreciate that the multiplexer multiplexes receiving lower data rate data, which is decimated four times in either receiving path, and control information introduced by the synchronization circuits SYNC 1 and SYNC2.

Claim 1 defines an analog-to-digital conversion contained in said integrated circuit, said converter producing data at a *relatively higher data rate*, also stated on page 5 lines 10-13 of the Applicant's specification. One of ordinary skill in the art of A/D conversion would appreciate that an analog-to-digital conversion always produces data at a relatively higher data rate at the output due to the nature of oversampling of an

analog-to-digital converter to avoid aliasing. Hence, the analog-to-digital converter in Gockler reference inherently reads the claimed limitation in light of the Applicant's specification.

- Applicant argues on page 3 that Gockler reference fails to teach an ADSL modem that allows data to be most efficiently shared between integrated circuits. In contrast, the ADSL modem claimed in claim 1 may achieve efficiency and cost reduction by providing a codec chip which transmits data externally off the chip when the data is at reduced or lower data rate. There is no teaching whatsoever as to this transmission at a reduced data rate externally off the chip, as claimed in claim 1.

Absence of other integrated circuits in claim 1 does not allow the claim to achieve intended purposes as stated in the argument. Furthermore, output data rate from the MUX is substantially reduced (e.g. four times) in the receiving path, see figure 2 in Gockler reference.

- Claim 14 is rejected for the same reason as stated above and in the last Office action. Furthermore, the method does not disclose transmit data between integrated circuit chips in the same modem. Hence, Gockler reference would also render all the limitations of claim 14 obvious since one of ordinary skill in the art would appreciate that output from the MUX is transmitted to another integrated circuit outside the modem.

Conclusion: In contrast with Applicant' argument, Gockler reference produces a prima facie case of obviousness not only on claims 1 and 14, but also on all of the rejected claims as stated in the last Office action. For reference purposes, below is the last office action recited again.

3. In addition to the previous rejection in the last Office action, new ground(s) of rejection is made in view of Mannering et al. U.S. Patent 6,404,804 B1 on claims 8-11 and 17-19.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8-10, 17-18, 23, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mannering et al. U.S. Patent 6,404,804 B1.

Regarding claims 8, 17 and 23, in column 8, line 45 column 9 line 6, figure 2 illustrates a modem 20 including an analog front end (AFE) 46, master DSP 22, and slave DSP 24. AFE 46, corresponding to the claimed first integrated circuit device, includes an analog-to-digital converter 46d for converting analog data from twisted pair 48 to a digital format suitable to present to parallel-to-serial (P/S) converter 46b, which serializes digital data. Data is then transmitted to

master DSP 22, corresponding to the claimed second integrated circuit device. Mannering et al. further discloses that DSP 22 and 24 communicate DSL frames to AFE 46, either sending or receiving. As appreciated by one of ordinary skill in the art, DSL frames include data and control information as claimed in pending patent application. Hence, parallel-to-serial (P/S) converter 46b incorporates data and control information in the serial data stream.

Mannering et al. does not expressly disclose the steps of decimating digital data rate and deserializing the data as claimed in the pending patent application. Decimating digital data after the analog-to-digital converter 46d has been known in the art of modem and has been cited in previous Office action. It would have been obvious for one of ordinary skill in the art at the time the invention was made that AFE 46 could be modified to include a decimator to decimate digital data, which is more suitable to present to parallel-to-serial (P/S) converter 46b. Furthermore, such modification would not change the principle operation of Mannering et al. modem. In regarding to de-serializing on the second integrated circuit, referring to figure 2, DSP 22 communicates with ISA bus through MBUS and 16-bit wide FIFO buffer 26 28. One of ordinary skill in the art will appreciate that serial data is de-serialized to parallel format in Master DSP 22.

Regarding claim 9, as well known in the art of DSL modem, discrete multi-tone modulation is employed in DSL modem.

Regarding claim 10, Master DSP 22 corresponds to the claimed second integrated circuit to provide digital signal processing.

Regarding claim 18, as recited in claim 17, DSP 22 communicates with ISA bus through MBUS and 16-bit wide FIFO buffer 26 28. One of ordinary skill in the art will appreciate that serial data is de-serialized to parallel format in Master DSP 22. The serial-to-parallel conversion process would increase the data rate as claimed.

Regarding claim 25, as recited in claim 8, Mannering et al. does not expressly disclose the steps of decreasing digital data rate using a decimator as claimed in the pending patent application. Nevertheless, decimating digital data after the analog-to-digital converter 46d has been known in the art of modem and has been cited in previous Office action. It would have been obvious for one of ordinary skill in the art at the time the invention was made that AFE 46 could be modified to include a decimator to decimate digital data, which is more suitable to present to parallel-to-serial (P/S) converter 46b. Furthermore, such modification would not change the principle operation of Mannering et al. modem.

5. Claims 11, 19, 24, 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mannering et al. U.S. Patent 6,404,804 B1 as applied to claims 9 and 18 and further in view of Ribner et al. U.S. Patent 6,028,891.

Regarding claim 11, as well known in the art, a discrete multi-tone, ADSL modem includes a fast fourier transform and a line decoder. The claimed features are shown in figure 1 of Ribner et al. US patent, which is incorporated here as a reference. Referring to figure 2 of Mannering et al. invention, AFE 46 does not include a fast fourier transform and a line decoder. In light of that reason, it would have been obvious for one of ordinary skill in the art that the Fast Fourier transform and a line decoder must reside in the Master DSP 22. It is not necessary to state a motivation because the claimed features are well known in the art of ADSL modem utilizing discrete multi-tone modulation.

Regarding claim 19, said claim is rejected using similar reasons as in claim 11 that the Fast Fourier transform and a line decoder must reside in the Master DSP 22.

Regarding claim 24, using similar argument as in claim 11, referring to figure 2, one of ordinary skill in the art will appreciate that Master DSP 22 would include a modulating circuit for generating DSL frames, see column 8, lines 45-65. Data rate is reduced due to conversion to serial data stream for transmission back through port Tx to serial-to-parallel (S/P) converter 46a of AFE 46. (S/P) converter 46a de-serializes DSL frames and the conversion process would increase the data rate. Mannering et al. does not expressly disclose the device that increases data rate. Nevertheless, increasing digital data by using an interpolator has been known in the art of modem and has been cited in previous Office action. It would have been obvious for one of ordinary

skill in the art at the time the invention was made that AFE 46 could be modified to include a interpolation filter for increasing the data rate. Furthermore, such modification would not change the principle operation of Mannering et al. modem.

Regarding claim 26, as recited in claim 24, one of ordinary skill in the art will appreciate that an interpolation filter can be implemented easily in AFE 46.

Regarding claim 27, using similar reason as in claim 19, an inverse Fast Fourier transform must reside in the Master DSP 22.

Regarding claim 28, splitterless modem is well known in the art DSL modem, hence, Mannering et al. modem is a splitterless modem.

Regarding 29, Mannering et al. further discloses that DSP 22 and 24 communicate DSL frames to AFE 46, either sending or receiving. As appreciated by one of ordinary skill in the art, DSL frames include data and control information as claimed in pending patent application. Hence, parallel-to-serial (P/S) converter 46b incorporates data and control information in the serial data stream.

Regarding claim 30, referring to figure 2, data is transmitted between AFE 46 and Master DSP 22 in both directions.

Examiner's Note: Below are the rejections of 1, 3-7, 14-16, 20-22 in the last Office action, which is incorporated below, because claims 1, 3-7, 14-16, 20-22 still stand rejected under 35 U.S.C 103(a).

Claim Rejections - 35 USC § 103

6. Claims 1, 3-7, 14-16, 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gockler et al. U.S. Patent 6,185,202 B1.

Regarding claim 1, Gockler et al. discloses in figure 2 a modem including an analog/digital converter ADU for converting a received analog data signal to a digital output signal at a relatively higher data rate as well known in the art, a decimator DE, corresponding to a device as claimed, coupled to the ADU with a fixed decimation factor 2 for obviously reducing the relatively higher data rate from the ADU to a lower data rate, a frequency splitter FWE and a downstream switch SWE for switching between one of two receive-signal paths, synchronization circuits SYNC1 and SYNC2 located in the two received paths, decoder DEC1 DEC2 located at the end of each receive-signal paths, and a multiplexer MUX for multiplexing the lower data rate through either one of synchronization circuits SYNC1 SYNC2. The lower data rate and control information are inherently multiplexed by the MUX. According to Gockler et al. teachings, signal transmission/reception takes place via only one of the two transmitting and receiving channels that are shown in figure 2. Gockler et al., however, does not specify the modem comprising an integrated circuit as claimed. Nevertheless, it would have been

obvious for one of ordinary skill in the art at the time of invention to implement the transmission and receive-signal paths in the modem onto an integrated circuit because modem components are always implemented on integrated circuit as it has been well known in the art.

Regarding claims 3 and 15, figure 2 shows the decimator DE with a fixed decimation factor 2, coupled to the analog/digital converter ADU.

Regarding claim 4, figure 2 further shows an analog anti-aliasing filter AAFE coupled to the ADU in turn coupled to the decimator DE in turn coupled to the MUX as claimed in the instant application.

Regarding claim 5, figure 2 further shows a demultiplexer DMUX coupled to digital interpolations IF1, IF2 with a variable interpolation factor through encoders ENC1 ENC2, a digital/analog converter DAU coupled to the IF1 and IF2 through a frequency splitter FWS. As well known in the art, the interpolation filter increases data rate of data received by an interpolation factor.

Regarding claim 6, figure 2 shows digital interpolations IF1, IF2 on both transmitted-signal paths with a variable interpolation factor coupled to the demultiplexer DMUX through encoders ENC1 ENC2.

Regarding claim 7, figure 2 shows both transmitted-signal paths and receive-signal paths.

Regarding claim 14, since claim 14 has similar scope with claim 1, the rejection argument of claim 1 also applies to claim 14. Furthermore, the multiplexing process serializes the data and the data is transmitted to another integrated circuit.

Regarding claim 16, as recited in claim 1 and 14, the data and control information are inherently multiplexed by the multiplexer MUX and the multiplexing process serialized the data as claimed in the instant application.

Regarding claim 20, figure 2 shows a demultiplexer DMUX receives digital data and the data rate is increased through either one of digital interpolations IF1 and IF2.

Regarding claim 21, as recited in claim 20, the digital interpolations IF1 and IF2 with variable interpolation factor increases the data rate.

Regarding claim 22, as shown in figure 2, the interpolated data is later on converted to analog format signal through the digital/analog converter (DAU).

Allowable Subject Matter

7. Claims 2, 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 703-305-2384. The examiner can normally be reached on Tuesday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 703-306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

MOHAMMAD H. GHAYOUR
PRIMARY EXAMINER